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| Form PTO 1449<br><br>U.S. Department of Commerce<br>Patent and Trademark Office<br><br>Information Disclosure Statement by Applicant | ATTY. DOCKET NUMBER<br><b>HITA.0501</b>     | SERIAL NUMBER<br><b>To be assigned</b> |
|  | APPLICANT<br><b>SAITO et al</b>             |  |
|  | FILING DATE<br><b>Concurrently herewith</b> | GROUP                                  |

**U.S. Patent Documents**

| Examiner<br>Initial | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE |
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**Foreign Patent Documents**

| Examiner<br>Initial | DOCUMENT NUMBER | FILING DATE | COUNTRY | CLASS | SUB-CLASS | TRANSLATION |    |
|---------------------|-----------------|-------------|---------|-------|-----------|-------------|----|
|                     |                 |             |         |       |           | Yes         | No |
| PC                  | 2002-313951     | 4/11/2001   | Japan   |       |           | Abstract    | X  |
|                     |                 |             |         |       |           |             |    |
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**Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)**

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| PC  | Digh Hisamoto, "FD/DG-SOI MOSFET - A Viable Approach to Overcoming the Device Scaling Limit", IEEE (2001), 4 pages   |
|   | Robert Chau et al., "30 nm Physical Gate Length CMOS Transistors with 1.0 ps n-MOS and 1.7 ps p-MOS Gate Delays", IEEE (2000), 4 pages   |
|   | Patrick P. Gelsinger, "Microprocessors for the New Millennium: Challenges, Opportunities, and New Frontiers", 2001 IEEE International Solid-State Circuits Conference, 10 pages                      |
|   | D.A. Buchanan et al. "80 nm Poly-silicon Gated n-FETs with Ultra-Thin Al <sub>2</sub> O <sub>3</sub> Gate Dielectric for ULSI Applications", IEEE (2000), 4 pages                                    |
|   | K. Torii et al., "Fixed Charge-Induced Mobility Degradation and its Recovery in MISFET's with Al <sub>2</sub> O <sub>3</sub> Gate Dielectric", IWGI 2001, Tokyo, pp. 230-232                         |
|   | K. Torii et al., "The Mechanism of Mobility Degradation in MISFETs with Al <sub>2</sub> O <sub>3</sub> Gate Dielectric", IEEE, 2002 Symposium on VLSI Technology Digest of Technical Papers, 2 pages |
|   | K. Rim et al., "Mobility Enhancement in Strained Si NMOSFETs with HfO <sub>2</sub> Gate Dielectrics", IEEE, 2002 Symposium on VLSI Technology Digest of Technical Papers, 2 pages                    |
|   | Kunihiro Suzuki et al., "Scaling Theory for Double-Gate SOI MOSFET's", IEEE Transactions on Electron Devices, Vol. 40, No. 12, December 1993, pp. 2326-2329  |
| PC  | International Technology Roadmap for Semiconductors, 2001 Edition, "Front End Processes", pp. 1-44   |
| EXAMINER  | /Phat Cao/   |
| DATE CONSIDERED   | 05/12/2006   |
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